

GaN integrated power amplifier O253SM7H



Vdd3 13 GND > 10 1 GND GND GND RFin 9 -[2] REquit GND $3 \leq GND$ Suitable for a variety of applications: GND 8 Microwave radio
Test measurement 5 4 6 /dd1

Overview

The O253SM7H is a GaN integrated power amplifier operating from 8 to 12 GHz. With a +28V operating voltage, it provides 22dB of power gain, 43dBm of saturated output power, and 38% power-added efficiency.

The amplifier adopts 7mmx7mm surface-mount non-leaded ceramic package, which can realize gas-tight encapsulation. The surface of the pin pad is processed by gold plating and is suitable for reflow soldering installation process.

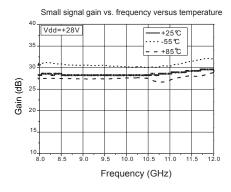
• Military and Aerospace • Instrumentation RF/microwave circuit Electrical Characteristics

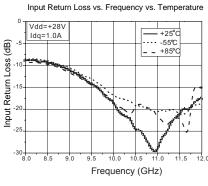
Application

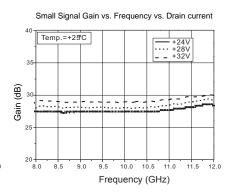
 $(TA = +25\%, Vdd=+28V, Vgg=-1.8V, Idq=0.6A, 50\Omega$ system, pulse width modulation PW = 100us, duty cycle DC = 10%)

symbol	Parameter	Min.	Тур.	Max.	Unit
Frequency	working frequency		8-12		GHz
Gain	Small signal gain	-	28	-	dB
Gp	Power gain (PIN=20dBm)	_	22	-	dB
IRL	Input return loss	_	10		dB
Pout	Output power (PIN=20dBm)		43		dBm
PAE	Power added efficiency (PIN=20dBm)		38		%
ldd	Working current (PIN=20dBm)	_	1.9	_	А

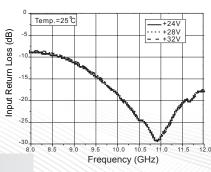
Test (Pulse operating conditions, drain modulation PW = 100us, duty cycle DC = 10%)



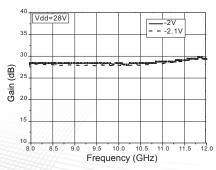




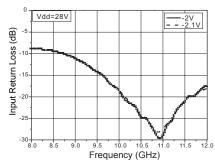
Input Return Loss vs. Frequency vs. Drain current



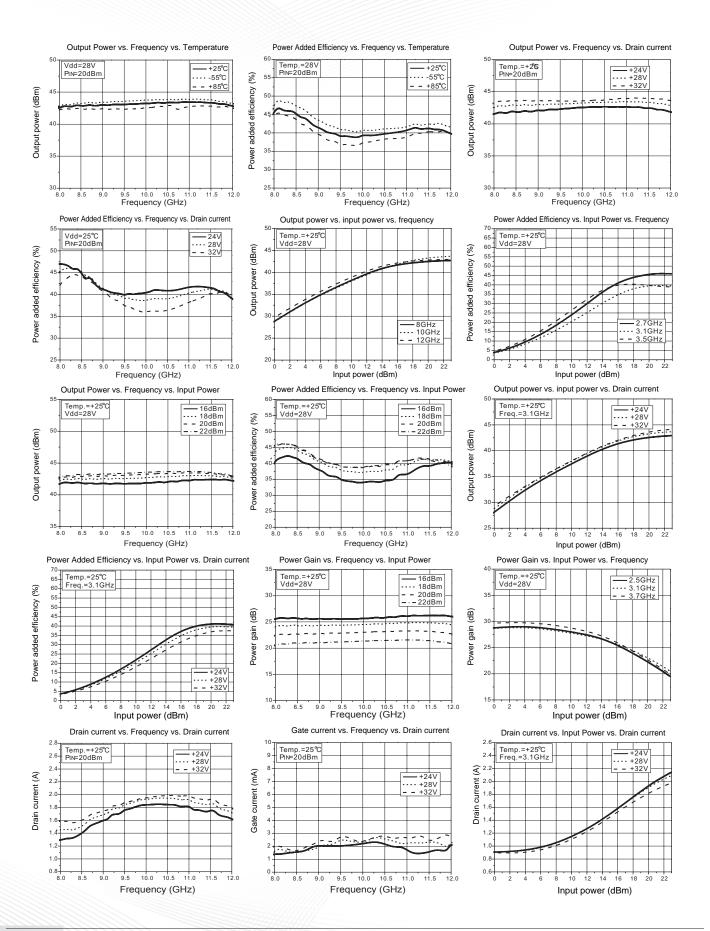




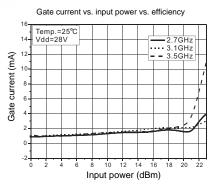
Input Return Loss vs. Frequency vs. Gate Voltage



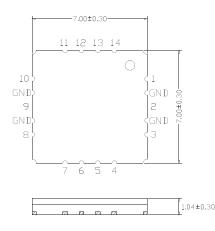




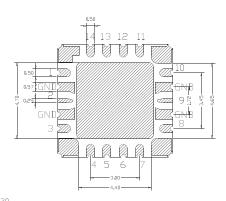




Di mensi ons



Input power (dBm)



Description:

- 1, Unit: mm
- 2, shell material: alumina ceramic
- 3, pin surface plating: nickel gold
- 4, the shell surface warping: less than 0.05mm
- 5, all ground pins please connect RF ground
- 6, The shell is suitable for reflow installation process

Limit parameter

Supply voltage (VDEVICE)	+33 V	
RF input power	+27dBm	
Storage temperature	-55~+125℃	
Operating temperature	-55~+85℃	



ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS

Vdd2

Vdd1

Pin definition

Pin.NO	Pin Name	Description	
9 RF in		RF input, external 50Ω system, no need for DC blocking capacitors	
2	RF out	RF output, external 50Ω system, no need for DC blocking capacitors	
4, 6, 14	Vdd	Amplifier drain bias	
12	V _{gg}	Amplifier gate bias requires external 1000pF and 1uF capacitors	
other	GND	The ground pin and the bottom of the shell need a large area to ground	

